GANPAT UNIVERSITY

FACULTY OF DIPLOMA ENGINEERING

Programme	Diploma Engineering				Branch/Spec.	Electronics and Communication Engineering			
Semester	VI				Version	1.0.0.0			
Effective from Academic Year	2026-27				Effective for the Batch admitted in	July 2024			
Course Code	1EC6101	Course Name			Semiconductor Packaging and Technology				
Teaching Scheme					Examination Scheme(Marks)				
(Per week)	Lecture(DT)		Practical(Lab.)		Total		CE	SEE	Total
	L	TU	P	TW					
Credit	3	0	0	0	3	Theory	40	60	100
Hours	3	0	0	0	3	Practical	--	--	--

Pre-requisites

Basics of VLSI Technology

Course Outcomes

On successful completion of the course, the students will be able to:

CO1	Acquire the fundamental knowledge of assembly and packaging process.
CO2	Understand the semiconductor package manufacturing process and materials.
CO3	Comprehend the Component and Package testing processes.
CO4	Analyze the methods of electrical and physical failure.

Theory Syllabus

Unit	Content	Hrs.
1	**Introduction:** History of IC's; Operation & Models for Devices of Interest: CMOS and MEMS, Introduction to Assembly flow, Functions of Electronic Packaging, Packaging Hierarchy, IC packaging: MEMS packaging, consumer electronics packaging, medical electronics packaging, Trends and Challenges, Driving Forces on Packaging Technology, Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging, Material for high density interconnect substrates.	12
2	**Package Manufacturing Process**: Package assembly process, wafer thinning, dicing, die attach, wire bonding, flip chip process, flux cleaning, underfill, encapsulation, laser marking, solder ball attach, reflow, singulation, IC packaging toolsets and equipment operation, clean room facility and operations, material used in packaging, die attached adhesive, underfill materials, bonding wires, wafer bumping, under-bump metallurgy, ceramics and glasses.	12
3	**Semiconductor Component and Package Test:** Overview of Testing methodologies, components tested and their characteristics, challenges in testing, types of testers (ATE and Benchtop testers), components and subsystems of testers, Principles of functional testing, parametric/ boundary scan, In-circuit test, flying probe test, test data analysis, design for testability ad tester calibration.	10
4	**Electrical and Physical Failure Analysis:** Package failure modes, failure detection mechanisms, failure analysis tools, test programs debugging, Electrical issues of systems packaging, signal distribution, power distribution, electromagnetic interference, transmission lines, clock distribution, nose sources, digital ad RF issues, interconnect capacitance, resistance and inductance fundamentals, packaging roadmaps – hybrid circuits, reliability test.	11

Practical Content

NA

Text Books

1	Tummala, Rao R., Fundamentals of Microsystems Packaging, McGraw Hill, 2001.

Reference Books

1	William Greig, Integrated Circuit Packaging, Assembly and Interconnections, Springer.
2	Silicon Technology Process, S K Gandhi, 2nd Edition, Wiley India,2009

3	Michael L. Bushnell &Vishwani D. Agrawal," Essentials of Electronic Testing for Digital, memory & Mixed signal VLSI Circuits", Kluwer Academic Publishers.2000.
4	Tummala, Rao R, Microelectronics packaging handbook, McGraw Hill, 2008.
ICT/MOOCsReference	
1	https://nptel.ac.in/courses/108108031
2	https://nptel.ac.in/courses/108104865

Mapping of CO with PO and PSO:															
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	2	1	1	2	0	0	0	0	1	0	2	2	1	1
CO2	3	3	3	2	2	0	0	0	1	1	1	2	1	2	2
CO3	2	2	1	2	1	0	0	0	0	1	0	2	2	1	1
CO4	3	1	2	2	1	0	0	0	0	1	0	3	1	2	2