

GANPAT UNIVERSITY									
FACULTY OF ENGINEERING & TECHNOLOGY									
Programme		Bachelor of Technology				Branch/Spec.		Electronics and Communication Engineering	
Semester		VII				Version		1.0.0.0	
Effective from Academic Year			2026-27			Effective for the Batch admitted in		July 2023	
Course Code		2EC71PE04		Course Name		Low Power VLSI Design			
Teaching Scheme					Examination Scheme (Marks)				
(Per week)	Lecture (DT)		Practical (Lab.)		Total		CE	SEE	Total
	L	TU	P	TW					
Credit	3	0	1	0	4	Theory	40	60	100
Hours	3	0	2	0	5	Practical	30	20	50
Pre-requisites									
Digital Electronics, CMOS VLSI Design									
Course Outcomes									
On successful completion of the course, the students will be able to:									
CO1	Understand basics of Power Dissipation.								
CO2	Learn low power circuit design and circuit level optimization.								
CO3	Acquire knowledge on SRAM								
CO4	Design low power circuit at submicron level								
Theory Syllabus									
Unit	Content								Hrs.
1	Power Dissipation In CMOS: Sources of power dissipation – Physics of power dissipation in MOSFET devices: The MIS structure, long channel MOSFET, Submicron MOSFET, gate induced drain leakage– Power dissipation in CMOS: short circuit dissipation, dynamic dissipation, load capacitance– Low power VLSI design: Limits – principles of low power design.								10
2	Design of Low Power Circuits: Transistor and Gate Sizing : Sizing an Inverter Chain, Transistor and Gate Sizing for Dynamic Power Reduction, Transistor Sizing for Leakage Power Reduction - Network Restructuring and Reorganization : Transistor Network Restructuring, Transistor Network Partitioning and Reorganization - Special Latches and Flip-flops: Self-gating Flip-flop, Varieties of Boolean Functions, Adjustable Device Threshold Voltage.								12
3	Synthesis For Low Power: Behavioral Level Transforms, Logic Level Optimization for Low power, Circuit Level Optimization.								06
4	Low Power Static Ram Architectures: Organization of a static RAM, MOS Static RAM Memory cell, Banked organization of SRAMs, Reducing voltage swings on bit lines, Reducing power in write driver circuits, Reducing power in sense amplifier circuits, method for achieving low core voltages from a single supply.								10
5	Design And Test Of Low Voltage CMOS Circuits: Circuit Design style, Leakage current in deep submicrometer transistors, Deep submicrometer device design issues, Low voltage circuit design techniques, Designing deep submicrometer ICs with elevated intrinsic leakage, multiple supply voltages.								07
Practical Content									
Practical assignments and tutorials are based on the above syllabus.									
Text Books									
1	K. Roy and S. C. Prasad, Low Power CMOS VLSI Circuit Design, John Wiley and Sons, 3 rd Edition, 2009.								
2	Jan Rabaey, Low Power Design Essentials, Springer Publications, 1 st Edition, 2009.								
Reference Books									
1	Chandrakasan and R. Brodersen, Low-Power CMOS Design, IEEE Press, 1 st Edition, 1995.								

2	Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Interscience, 2000.
ICT/MOOCs Reference	
	https://nptel.ac.in/courses/106105034
	https://www.youtube.com/watch?v=zoz5uFT14FA

Mapping of CO with PO and PSO:															
	P O 1	P O 2	P O 3	P O 4	P O 5	P O 6	P O 7	P O 8	P O 9	P O 10	P O 11	P O 12	P S O 1	P S O 2	P S O 3
CO1	2	2	1	1	1	0	0	0	2	0	0	0	2	1	1
CO2	3	3	3	2	1	0	0	0	2	0	0	0	1	2	2
CO3	2	2	3	2	2	2	0	0	2	0	0	2	2	1	1
CO4	2	2	3	0	2	0	2	0	2	0	0	3	1	2	2