GANPAT UNIVERSITY									
FACULTY OF ENGINEERING & TECHNOLOGY									
Programme	Master of Technology					Branch/Spec.	Electronics and Communication Engineering – VLSI System Design		
Semester	I					Version	1.0.0.1		
Effective from Academic Year		2023-24				Effective for the Batch admitted in		July 2023	
Course Code	3EC1111	Course Name				Digital VLSI Design			
Teaching Scheme						Examination Scheme (Marks)			
(Per week)	Lecture(DT)		Practical(Lab.)		Total		CE	SEE	Total
	L	TU	P	TW					
Credit	3	0	1	-	4	Theory	40	60	100
Hours	3	0	2	-	5	Practical	30	20	50

Pre-requisites
Digital Electronics

Course Outcomes	
On successful completion of the course, the students will be able to:	
CO1	Understand the design and simulate digital circuit
CO2	Students will analyze the fundamentals of digital design and how each digital system works
CO3	Evaluate the Finite state machine implementation
CO4	Understand the various VLSI design styles

Theory Syllabus

Unit	Content	Hrs.
1	**Introduction:** Number System and its applications, Logic Gates, Universal Gates, Design of various gates using universal gates,	6
2	**Combinational Logic Design (Part I):** Introduction, Logic gates and Synthesizable RTL, Arithmetic Circuits, Design of circuits, Optimization of logic circuit.	8
3	**Combinational Logic Design (Part II):** Multiplexer, Decoder, Encoders, Design of logic circuits using Multiplexers and Demultiplexers, Applications of Encoders and Decoders, case study	8
4	**Sequential Logic Design** Introduction, Flip Flop, Synchronous and Asynchornous reset, Counters design, Shift registers, Timing and Performance Evaluation, Memory Module Design.	7
5	**Asynchronous Sequential Logic:** Analysis Procedure, Circuits with latches, Design procedure, Reduction of state and flow tables, Race-free state assignment, Hazards, Design examples.	8
6	**Finite State Machines:** Moore vs Melay machine, FSM Encoding Styles, One Hot Encoding, Sequence Detectors using FSMs, Sequence detector using Melay Machine, Improving design performance for FSMs.	8

Practical Content

Practical, assignments and tutorials are based on above syllabus.

- Tools used during laboratory works: CVER, VCS, Design Vision, Design Compiler.
- Implementation of all the designs taught using Verilog HDL

Text Books

1	Contemporary logic design by R. Katz, 2nd Edition, Prentice Hall 2004.
2	A.Chandrakasan, et al., Design of High-Performance Microprocessor Circuits, IEEE Press, 2001 - D. Harris, Skew-tolerant Circuit Design, Morgan Kaufmann, 2000. - K. Bernstein, et al., High Speed CMOS Design Styles, Kluwer Academic Publishers , 1998. - N. Weste and D. Harris, CMOS VLSI Design, Addison-Wesley, 4th edition, 2010.

3	Fundamentals of Logic Design by Charles H. Roth, Jr. Larry L. Kinney 7 Edition, Cengage Learning, 2013.
Reference Books	
1	Switching and finite automata by Zvikohavi and Niraj Jha, 3rd Edition, Cambridge 2010.
2	Digital Design - Principles & Practices by J. F. Wakerly. 4th Edition, Pearson, 2005.
ICT/MOOCs Reference	
1	https://www.youtube.com/watch?v=PUB1goqGtRQ
2	https://www.youtube.com/watch?v=rziANtQwFUw

Mapping of CO with PO and PSO :															
Cos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	1	2	3	3	3	2	3	2	2	2	3	1	1	1	2
CO2	2	2	2	2	2	3	2	3	3	3	2	2	2	2	1
CO3	3	3	3	3	3	2	2	3	3	2	2	1	1	1	2
CO4	3	1	3	3	2	2	3	1	3	2	2	3	3	2	2