GANPAT UNIVERSITY

FACULTY OF DIPLOMA ENGINEERING

Programme	Diploma in Electronics and Communication Engineering		
Semester	IV	Version	1.0.0.0
Effective from Academic Year	2025-26	Effective for the batch Admitted in	JULY 2025
Course code	1EC4103	Course Name	Digital VLSI Design

I.TEACHING-LEARNING AND ASSESSMENT SCHEME

Course Type	Course Code	Learning Scheme						Assessment Scheme										
		Actual Contact Hrs./Week			SLH	NLH	Credits	Theory				Practical				Based on SL		Total Marks
		CL	TL	LL				FA-TH	SA-TH	TOTAL		FA-PR	SA-PR	TOTAL		SLA		
								MAX	MAX	MAX	MIN	MAX	MAX	MAX	MIN	MAX	MIN	
SEC	1EC4103	3	-	2	3	8	4	40	60	100	40	30	20	50	20	20	8	170

Abbreviation:	**CL-** Classroom Learning	**TL -** Tutorial Learning	**LL -** Laboratory Learning
	SLH - Self Learning Hours	**NLH -** Notional Learning Hours	**SLA -** Self Learning Assessment
	FA - Formative Assessment (Term work +Mid Sem Exam +Attendance)		**SA -** Summative Assessment

II. PRE-REQUISITES

Semiconductor physics, Analog electronics, Electronic devices and circuits

III. INDUSTRY / EMPLOYER EXPECTED OUTCOMES

To introduce VLSI design concepts and digital system design styles & to understand MOS transistor operation and inverter design. Design combinational and sequential MOS logic circuits and to understand fabrication technology and semiconductor memory architectures.

IV. COURSE LEARNING OUTCOMES

At the end of the course, students will be able to achieve the following course learning outcomes:

CO1: Explain VLSI design flow and MOS transistor characteristics.

CO2: Design combinational and sequential MOS logic circuits.

CO3: Analyze MOSFET fabrication and inverter layouts.

CO4: Compare different semiconductor memory architectures

V. THEORY LEARNING OUTCOMES AND ALIGNED COURSE CONTENT:

Name of Unit	Theory Learning outcomes (TLO's) aligned to CO's	Learning Content mapped with Theory Learning outcomes (TLO's) & CO's	Marks	Hours
Unit-1 Digital System and MOS Transistor	**TLO 1.1:** Understand the VLSI design flow and explain the sequence of steps involved in the development of VLSI systems. **TLO 1.2:** Explain the Y-Chart model and its role in representing behavioral, structural, and physical design domains. **TLO 1.3:** Understand the concept of design hierarchy and decomposition and explain its importance in managing complex VLSI designs. **TLO 1.4:** Explain the MOS structure and its operation under different biasing conditions. **TLO 1.5:** Analyze the current–voltage (I–V) characteristics of MOSFETs and identify different	1.1 VLSI Design Flow 1.2 Y-Chart 1.3 Design Hierarchy and Decomposition 1.4 MOS Structure and Operation 1.5 MOSFET I–V Characteristics	**8**	**10**

	regions of operation.			
Unit-2 **MOS Inverters**	**TLO 2.1:** Understand the concept and working principle of MOS inverters used in digital VLSI circuits. **TLO 2.2:** Explain the operation and characteristics of a resistive load MOS inverter. **TLO 2.3:** Describe the operation of an inverter with n-type MOSFET load and analyze its voltage transfer behavior. **TLO 2.4:** Explain the working of an enhancement-mode load NMOS inverter and its performance characteristics. **TLO 2.5:** Describe the operation of a depletion-mode load NMOS inverter and discuss its advantages over enhancement-mode load inverter. **TLO 2.6:** Compare enhancement-load and depletion-load NMOS inverters in terms of switching characteristics and power dissipation. **TLO 2.7:** Explain the circuit operation and characteristics of a CMOS inverter, including noise margins and power consumption.	2.1 MOS Inverter : concept and working, 2.2 Resistive load Inverter 2.3 Inverter with n-type MOSFET Load 2.4 Enhancement load NMOS 2.5 Depletion Load NMOS 2.6 Enhancement load and Depletion Load NMOS 2.7 CMOS Inverter: Circuit operation and description	**12**	**9**
Unit-3 **Combinational MOS Logic Circuits**	**TLO 3.1:** Explain the operation of MOS logic circuits using depletion-load nMOS and analyze their suitability for combinational logic implementation. **TLO 3.2:** Design and analyze two-input NOR and NAND gates using CMOS logic and compare their performance with nMOS implementations. **TLO 3.3:** Analyze and implement complex CMOS logic circuits using Euler path, AOI, and OAI gate structures for optimized layout design **TLO 3.4:** Explain the pseudo-nMOS logic style, its working principle, advantages, limitations, and applications in VLSI circuits. **TLO 3.5:** Design and analyze a CMOS full adder circuit and evaluate its logic operation and performance. **TLO 3.6:** Explain the operation and applications of CMOS transmission gates in	3.1 MOS Logic circuits with Depletion nMOS loads 3.2 CMOS Logic circuits: Two input NOR & NAND gate 3.3 Complex logic circuits, Euler path, AOI, OAI gates 3.4 Pseudo nMOS gate 3.5 CMOS full adder circuit 3.6 CMOS transmission gate 3.7 CPL.	**12**	**8**

	combinational logic and data path circuits. **TLO 3.7:** Explain the concept of CPL			
Unit-4 Sequential MOS Logic Circuits:	**TLO 4.1:** Explain the behavior of bistable elements and their role in storing binary information in sequential MOS logic circuits. **TLO 4.2:** Describe the SR latch circuit, its operation, truth table, invalid state, and applications in digital systems. **TLO 4.3:** Understand the concepts of clocked latches and flip-flop circuits, highlighting the importance of clock signals in sequential logic**.** **TLO 4.4:** Explain the CMOS D latch, its circuit implementation, operation, and timing behavior**.** **TLO 4.5:** Describe the working of edge-triggered flip-flops, including timing parameters such as setup time, hold time, and clock edge operation.	4.1 Behavior of Bistable Elements 4.2 SR Latch Circuit 4.3 Clocked Latch and Flip-Flop Circuits concepts. 4.4 CMOS D Latch 4.5 Edge-Triggered Flip-Flop	**16**	**9**
Unit-5 : Fabrication Of MOSFETS	**TLO 5.1:** Understand the concept and significance of MOSFET fabrication technology in VLSI integrated circuits. **TLO 5.2:** Explain the MOSFET fabrication process flow, including the basic steps such as oxidation, diffusion, ion implantation, lithography, and metallization. **TLO 5.3:** Describe the step-by-step fabrication of an NMOS transistor and explain the function of each fabrication stage. **TLO 5.4:** Explain the LOCOS (Local Oxidation of Silicon) technique used for device isolation in MOS technologies. **TLO 5.5:** Understand the Shallow Trench Isolation (STI) technique and compare it with LOCOS for advanced CMOS processes. **TLO 5.6:** Describe the CMOS n-well fabrication process and explain its importance in CMOS circuit realization. **TLO 5.7:** Apply layout design rules to ensure proper fabrication, reliability, and manufacturability of VLSI circuits. **TLO 5.8:** Design a CMOS inverter layout following standard layout design rules. **TLO 5.9:** Draw and interpret stick diagrams of NMOS, PMOS, and CMOS circuits for effective layout planning.	**5.1** Fabrication Of MOSFETS: **5.2** Fabrication Process flow: basic steps **5.3** Fabrication of NMOS transistor **5.4** Device isolation techniques: LOCOS **5.5** STI **5.6** CMOS nWell process **5.7** Layout design rules **5.8** CMOS inverter layout design **5.9** stick diagram of NMOS PMOS CMOS.	**12**	**9**

Unit-6 Semiconductor Memories:	**TLO 6.1:** Understand the basic concept, classification, and characteristics of DRAM used in semiconductor memory systems. **TLO 6.2:** Explain the operation of a 1-transistor DRAM (1T-DRAM) cell, including read, write, and refresh operations. **TLO 6.3:** Describe the structure, operation, and characteristics of SRAM and compare it with DRAM. **TLO 6.4:** Explain the working of a full CMOS SRAM cell, including storage mechanism and stability considerations. **TLO 6.5:** Understand the concept and types of non-volatile memories and their applications in digital systems.	6.1 DRAM 6.2 Operation of 1-transistor DRAM cell 6.3 SRAM 6.4 Full CMOS SRAM cell 6.5 Non-volatile memory		

VI. LABORATORY LEARNING OUTCOME AND ALIGNED PRACTICAL			
Sr. No.	**Practical/Laboratory Learning Outcome (LLO)**	**Practical Titles**	**Relevant COs**
1	**LLO 1.1:** Understand and simulate the VLSI design flow using basic CAD tools.	Study of VLSI Design Flow and introduction to VLSI CAD tools.	CO1
2	**LLO 2.1:**Analyze the voltage transfer characteristics of MOS inverters using simulation tools	Simulation and analysis of Resistive Load MOS Inverter characteristics.	CO1
3	**LLO 3.1:** Design and simulate NMOS and CMOS logic gates (NAND, NOR) and verify their functionality.	Simulation and analysis of NMOS Inverter with Enhancement and Depletion Load.	CO1
4	**LLO 4.1:** Implement and analyze complex CMOS logic circuits including AOI and OAI gates.	Design and simulation of CMOS Inverter and study of voltage transfer characteristics.	CO3
5	**LLO 5.1:** Design and simulate a **CMOS** full adder circuit and verify its logic operation.	Analysis of Cascaded CMOS Inverters and propagation delay.	CO4
6	**LLO 6.1:** Analyze the operation of latches and flip-flops using simulation tools.	Design and simulation of Two-input NAND and NOR gates using NMOS logic.	CO2
7	**LLO 7.1:** Design and simulate master–slave and edge-triggered flip-flops and study timing parameters.	Design and simulation of Two-input NAND and NOR gates using CMOS logic.	CO2
8	**LLO 8.1:** Apply layout design rules to create a CMOS inverter layout.	Design and simulation of Complex CMOS Logic Circuits (AOI / OAI gates).	CO4
9	**LLO 9.1:** Draw and interpret stick diagrams for NMOS, PMOS, and CMOS circuits.	Design and simulation of CMOS Full Adder Circuit.	CO3
10	**LLO 10.1:** Study and analyze the operation of SRAM and DRAM cells using circuit diagrams or simulations.	Simulation and analysis of CMOS Transmission Gate.	CO4

VII. SUGGESTED MICRO PROJECT / ASSIGNMENTS / ACTIVITIES FOR SELF LEARNING / SKILL DEVELOPMENT (SELF LEARNING)

A. Self-Learning Assignments / Activities

1. **VLSI Design Flow Chart Preparation**
   Prepare a detailed chart or PPT explaining the complete VLSI design flow from system specification to fabrication.
2. **Comparative Study of VLSI Design Styles**
   Prepare a report comparing **FPGA, Gate Array, Standard Cell, and Full Custom Design** in terms of cost, performance, power, and applications.
3. **MOS Inverter Analysis Assignment**
   Analyze resistive load, NMOS load, and CMOS inverters with respect to voltage transfer characteristics and power dissipation.
4. **Logic Gate Design Using CMOS**
   Design CMOS implementations of basic logic gates and explain their working with truth tables.
5. **Flip-Flop Timing Diagram Assignment**
   Draw and explain timing diagrams for SR latch, D latch, master–slave flip-flop, and edge-triggered flip-flop.
6. **Fabrication Process Study**
   Prepare a short report on MOSFET fabrication steps including oxidation, diffusion, ion implantation, and metallization.

B. Mini Projects (Skill Development Focused)

1. **Design and Simulation of CMOS Full Adder**
   Design and simulate a CMOS full adder using VLSI CAD tools and analyze its performance.
2. **CMOS Inverter Layout Design Project**
   Design the layout of a CMOS inverter following layout design rules and prepare stick diagrams.
3. **Implementation of AOI / OAI Logic Circuits**
   Design and simulate AOI or OAI logic circuits and verify their functionality.
4. **Design of SRAM Cell**
   Design and analyze a **6T CMOS SRAM cell** and study its read and write operations.
5. **Sequential Circuit Design Project**
   Design and simulate a master–slave or edge-triggered flip-flop and analyze timing parameters.
6. **Memory Decoder Design**
   Design row and column decoders used in semiconductor memory architectures.

VIII. LIST OF INSTRUMENTS / EQUIPMENT / TRAINER BOARD	
1	VLSI CAD Software (Cadence / Microwind / Tanner / LTspice)
2	Desktop Computer System Required for executing VLSI design and simulation tools.
3	MOSFET Trainer Kit Used to study MOSFET characteristics and basic device operation.
4	CMOS Logic Trainer Board Used to verify CMOS inverter and logic gate functionality.
5	Memory Trainer Kit (SRAM / DRAM) Used to study memory cell operations and decoding logic

IX. LIST OF REFERENCE BOOKS			
Sr.No.	**Title**	**Author**	**Publication**
1	CMOS Digital Integrated Circuits	Sung-Mo Kang & Yusuf Leblebici	TMH
2	Modern VLSI Design	Wayne Wolf	Pearson Education
3	Basic VLSI Design	Douglas A. Pucknell & Kamran Eshraghian	PHI
4	Digital Integrated Circuits	Jan M. Rabaey	Pearson Education
5	VLSI Design	K. Lal Kishore	Pearson Education

X. LINK OF LEARNING WEB RESOURCE	
1	https://nptel.ac.in/courses/117106092
2	https://onlinecourses.nptel.ac.in/noc21_ee09/preview
3	https://www.allaboutcircuits.com
4	https://www.vlsiuniverse.com

XI. SUGGESTED WEIGHTAGE TO LEARNING EFFORTS & ASSESSMENT PURPOSE

Unit	Unit Title	Aligned COs	Learning Hours	R-Level	U-Level	A-Level	Total Marks
1	Digital System and MOS Transistor	CO1	10	3	4	3	10
2	MOS Inverters	CO2	9	3	4	4	11
3	Combinational MOS Logic Circuits	CO2	8	5	6	5	16
4	Sequential MOS Logic Circuits	CO2	9	4	3	4	11
5	Fabrication of MOSFETs & Memories	CO3, CO4	9	3	5	4	12
		Grant Total	**45**	**18**	**22**	**20**	**60**

XII. COs AND POs AND PSOs MAPPING

Course outcome (Cos)	Programme Outcomes (POs)							Programme Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
CO1	3	3	2	0	0	0	0	2	1	1
CO2	3	3	3	1	0	0	1	3	2	3
CO3	3	3	2	0	0	1	1	2	3	2
CO4	3	2	3	1	0	0	0	2	2	2

Legends: - *3- High 2-Moderate/Medium 1-Slight/Low 0-None*