



**Ganpat University**  
॥ विद्यया समाजोत्कर्षः ॥

Faculty of  
**Computer Applications**



|   |   |     |                         |     |  |                       |           |            |              |
|---|---|-----|-------------------------|-----|--|-----------------------|-----------|------------|--------------|
| <b>Programme</b>  | BCA Honors (Cyber Security)   |     |                         |     | <b>Branch</b>                              | Computer Applications |           |            |              |
| <b>Semester</b>   | I   |     |                         |     | <b>Version</b>                             | 1.0.0.0               |           |            |              |
| <b>Effective from Academic Year</b>   |   |     | 2026-2027               |     | <b>Effective for the batch Admitted in</b> |                       |           | June 2026  |              |
| <b>Subject Code</b>   | U101B3DL  |     | <b>Subject Name</b>     |     | DIGITAL LOGIC                              |                       |           |            |              |
| <b>Teaching scheme</b>  |   |     |                         |     | <b>Examination scheme (Marks)</b>          |                       |           |            |              |
| <b>(Per week)</b>   | <b>Lecture (DT)</b>   |     | <b>Practical (Lab.)</b> |     | <b>Total</b>                               |                       | <b>CE</b> | <b>SEE</b> | <b>Total</b> |
|   | L   | TU  | P                       | TW  |  |                       |           |            |              |
| Credit  | 4   |     | -                       | -   | 4  | Theory                | 50        | 50         | 100          |
| Hours   | 4   |     | -                       | -   | 4  | Practical             | -         | -          | -            |
| <b>Objective:</b>   |   |     |                         |     |  |                       |           |            |              |
| To provide students with a foundational understanding of the principles and techniques underlying digital systems.  |   |     |                         |     |  |                       |           |            |              |
| <b>Pre-requisites:</b>  |   |     |                         |     |  |                       |           |            |              |
| students have a solid foundation in mathematics, logic, and basic engineering principles, which are essential for comprehending the concepts covered in a Digital Logic course. |   |     |                         |     |  |                       |           |            |              |
| <b>Course Outcomes :</b>  |   |     |                         |     |  |                       |           |            |              |
| <b>Name of CO</b>   | <b>Description</b>  |     |                         |     |  |                       |           |            |              |
| C01   | Translate various codes and number systems utilized in digital communication and computer systems.  |     |                         |     |  |                       |           |            |              |
| C02   | Utilize circuits for converting codes and number systems, and analyze and contrast various logic families, the fundamental components of distinct logic gates, in terms of economic factors, performance, and efficiency. |     |                         |     |  |                       |           |            |              |
| C03   | Simplifying and Implementation at the Gate Level  |     |                         |     |  |                       |           |            |              |
| C04   | Gain the capability to create and evaluate combinational logic circuits.  |     |                         |     |  |                       |           |            |              |
| C05   | Develop the proficiency to create and assess sequential logic circuits.   |     |                         |     |  |                       |           |            |              |
| <b>Mapping of CO and PO</b>   |   |     |                         |     |  |                       |           |            |              |
| Cos   | PO1   | PO2 | PO3                     | PO4 | PO5  | PO6                   | PO7       | PO8        |              |
| C01   | 3   | 2   | 1                       | 0   | 0  | 1                     | 1         | 1          |              |
| C02   | 3   | 3   | 2                       | 2   | 0  | 1                     | 1         | 1          |              |
| C03   | 3   | 3   | 3                       | 2   | 0  | 1                     | 1         | 1          |              |
| C04   | 3   | 3   | 3                       | 2   | 1  | 1                     | 1         | 1          |              |
| C05   | 3   | 3   | 3                       | 2   | 1  | 1                     | 1         | 1          |              |
| <b>Content:</b>   |   |     |                         |     |  |                       |           |            |              |
| <b>Unit</b>   |   |     |                         |     |  |                       |           |            | <b>Hrs</b>   |

|   |  |    |
|---|--|----|
| 1 | <b>Foundations of Digital Systems and Number Systems</b><br>Digital system overview, Introduction to binary numbers, Number base conversion techniques, Positional number system, Binary, Octal, Hexadecimal, and Decimal number systems, Representation of signed numbers and signed magnitude, Binary arithmetic operations: Addition, Subtraction, Multiplication, Division   | 12 |
| 2 | <b>Boolean Algebra and Basic Logic Gates</b><br>Introduction to Boolean algebra, Addition and Multiplication in Boolean algebra, Binary logic functions exploration, Logic gates and Truth tables overview, Basic logic gates: AND, OR, NOT, Universal gates: NAND and NOR, EX-OR and EX-NOR logic gates, Boolean rules and Laws, De-Morgan's theorem  | 12 |
| 3 | <b>Gate Level Minimization and Realization</b><br>Realization of switching functions using logic gates, Canonical forms and Standard forms, Sum of product and Product of sum forms, Realization of Boolean functions using universal gates, The map method: Three-variable map and Four- variable map, Logic expression simplification with grouping cell, Quine-McClusky method, Realization of combinational circuits using truth tables  | 12 |
| 4 | <b>Analysis and Design of Combinational Circuits</b><br>Introduction to combinational circuits, Binary Adders: Half adder, Full adder, Binary Subtractors: Half Subtractor, Full Subtractor, Parallel binary adder, Binary comparator or Magnitude comparator, Decoders and Encoders, Multiplexers and Demultiplexers, Parity generator and Parity checkers, Code converter  | 12 |
| 5 | <b>Sequential Logic, Counters, and Registers</b><br>Latches: Active High S-R Latch, Active Low S-R Latch, Gated S-R Flip-Flop, D-flip-flop, Edge-triggered flip-flops: S-R FF, D-ff, J-K flip-flop, Race condition in flip-flops, Master-slave J-K flip-flop, Introduction to counters: Three-bit, synchronous counter, Four-bit asynchronous counter, ripple counter, Synchronous binary up counters: Three-bit and Four-bit, Synchronous binary down counters: Three-bit and Four-bit, Serial In and Serial Out register, Universal Shift register | 12 |

**Practical Content:**

Not Applicable

**Text Books:**

1 Fundamentals of Computers by V. Raja Raman

**Reference Books:**

1 Digital Design, M. Morris Mano, Pearson education.

2 Digital Circuit and Designs -S. Alivahanan, S. Arivazhagan - Vikash Publications.

3 Modern Digital Electronics: R. P Jain.

**Web References / MOOC / Certification Course**

1 <https://www.coursera.org/learn/digital-systems>

2 <https://www.udemy.com/course/digitalelectronics/?couponCode=ST12MT030524>

3 [https://onlinecourses.nptel.ac.in/noc22\\_ee55/preview](https://onlinecourses.nptel.ac.in/noc22_ee55/preview)

4 <https://www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/>

5 <https://www.javatpoint.com/digital-electronics>

|   |   |
|---|---|
| 6 | <a href="https://www.tutorialspoint.com/digital_circuits/index.htm">https://www.tutorialspoint.com/digital_circuits/index.htm</a> |
| 7 | <a href="https://www.geeksforgeeks.org/what-is-digital-logic/">https://www.geeksforgeeks.org/what-is-digital-logic/</a>           |

**Question Paper Scheme:**

**End Semester Examination Duration:** (2 Hours Theory Examination)

**Note for Examiner:** -

Q-1 Any Five out of Seven (25 Marks)

Q-2 Any Two out of Three (06 Marks)

Q-3 Mandatory question (05 Marks)

Q-4 Any Two out of Three (08 Marks)

Q-5 Any Two out of Three (06 Marks)

*The question paper must comprehensively address all Course Outcomes (COs), align Taxonomy levels, and ensure complete syllabus coverage.*