Ganpat University
॥ विद्यया समाजोत्कर्षः ॥

Faculty of Computer Applications

Programme	B.Sc. IT Honours (Artificial Intelligence & Machine Learning)	**Branch**	Computer Applications
Semester	I	**Version**	1.0.0.0
Effective from Academic Year	2026-27	**Effective for the batch Admitted in**	June 2026
Subject code	U81B3DE	**Subject Name**	DIGITAL ELECTRONICS

Teaching scheme

(Per week)	Lecture (DT)		Practical (Lab.)		Total	Examination scheme (Marks)	CCE	SEE	Total
	L	TU	P	TW					
Credit	2	-	2	-	4	Theory	50	50	100
Hours	2	-	4	-	6				

Objective:

To acquire knowledge of Digital electronic circuits and its components

Pre-requisites:

Basic concepts of mathematics

Learning Outcome:

Name of CO	Description
CO1	Learn different number system, understand number representation and conversion between different number system in digital electronic circuit and perform number conversion
CO2	Using logic gates it helps how to design and implement digital logic circuit in the system.
CO3	Implement Boolean relation and with the use of it solve the karnaugh map simplification.
CO4	Solve and implement the combinational circuit as well as sequential circuit and how to implement in design digital logic circuit.
CO5	Understand different types of memory, use of different registers in digital circuits to hold information and analyze complex inputs of several types of flip-flop devices.

Mapping of CO and PO:

Cos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	0	2	0	1	1	2	2	3	0	2	2	1
CO2	2	1	2	3	2	2	2	2	0	2	2	2
CO3	1	2	2	2	1	2	3	2	0	2	3	2
CO4	3	2	3	2	2	3	3	2	0	3	3	3
CO5	2	1	2	2	1	2	1	2	0	1	1	1

Content:

Unit	Content	Hrs.
1	**Data Representation and Number System** Number Systems: Introduction to Decimal, Binary, Octal, Hexadecimal Number Systems, Conversation of number from one number system to another number System, Binary Arithmetic: Addition, Subtraction (Simple method, using 1's And 2's Complement method), Representation & Error detection and correction codes	06
2	**Logic Gates and Boolean algebra:** **Logic Gates**	06

	Introduction of Digital Electronics, Inverter, OR Gate, AND Gate, NOR Gate, NAND Gate , Demorgan's Theorems, EX-OR Gate, EX-NOR Gate **Boolean algebra:** Boolean Relation, Universal Building blocks (Only for Logic conversion, not for theory), Implementation of Digital circuits using Universal gates, Pair, Quad, Octet, K-MAP Simplifications	
3	**Data Processing Circuit and ALU** **Data Processing Circuits:** Combinational circuits and sequential circuits, Multiplexer (4 to 1, 8 to 1,16 to 1), Demultiplexer (1 to 4, 1 to 8, 1 to 16) [02], Decoder (1 of 4, 1 of 8,1 of 16) Seven Segment Display, Decoder (1 of 4, 1 of 8, 1 of 10, BCD to Decimal) [02], Encoder (Decimal to BCD, Hexadecimal to BCD) **Arithmetic Logic Unit:** Half Adder, Full Adder, Half Subtractor, Binary Adder	06
4	**Flip-Flop, Memory, Register, Counter** **Flip Flop, Memory** NOR Latch, NAND Latch, R S Flip Flop, ROM, PROPM (Programmable ROM) , EPROM (Erasable Programmable ROM), EEPROM (Electrically Erasable programmable ROM), RAM, Dynamic RAM, Static RAM, Hexadecimal Addresses	06
5	**Registers and counters** Buffer Register, Shift left register, Shift right register, Asynchronous and Synchronous Counter(Ring Counter, Ripple Counter)	06

Practical Content:	
List of programs specify by subject teacher based on above mention topics	
Reference Books:	
1	Digital Computer Electronics by Malvino & Brown, Third Edition – TMH, Publications
2	Fundamentals of computer by V.Rajaraman-PHI Publications.
3	Digital Principles and applications by Malvino & Leach – TMH Publication.
Web Reference:	
1	https://www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/
MOOC/Certificate Course:	
1	https://www.classcentral.com/course/youtube-digital-electronics-48205
2	https://onlinecourses.swayam2.ac.in/cec21_cs16/preview
3	https://www.udemy.com/course/introduction-to-digital-electronics/
4	https://www.classcentral.com/course/youtube-digital-electronics-for-gate-54061
Question Paper Scheme:	
	End Semester Examination Duration: (2 Hours Theory Examination) **Note for Examiner: -** Q-1 Any Five out of Seven (25 Marks) Q-2 Any Two out of Three (06 Marks) Q-3 Mandatory question (05 Marks) Q-4 Any Two out of Three (08 Marks) Q-5 Any Two out of Three(06 Marks) *The question paper must comprehensively address all Course Outcomes (COs), align with Bloom's Taxonomy levels, and ensure complete syllabus coverage.