GANPAT UNIVERSITY

FACULTY OF DIPLOMA ENGINEERING

Programme	Diploma in Electrical Engineering		
Semester	III	Version	1.0.0.0
Effective from Academic Year	2026-27	Effective for the batch Admitted in	JULY 2025
Course code	1EE3105	Course Name	Digital Electronics and Microprocessor

I. TEACHING-LEARNING AND ASSESSMENT SCHEME

Course Type	Course code	Course Title	Teaching & Learning Scheme									Examination Scheme							
			Credit				Actual Contact Hrs/week			SLH	Total Learning Hrs/Week	TH			PR			SLA	Total
			CL	TL	LL	Total	CL	TL	LL			CE	SEE	Total	CE	SEE	Total		
DSC	1EE3105	Digital Electronics and Microprocessor	3	0	1	4	3	0	2	3	8	40	60	100	30	20	50	20	170

Abbreviation:	**CL-** Classroom Learning	**TL -** Tutorial Learning	**LL -** Laboratory Learning
	SLH - Self Learning Hours	**SLA -** Self Learning Assessment	**SA -** Summative Assessment
	CE – Continuous Evaluation		**SEE –** Semester End Examination

II. PRE-REQUISITES

None.

III. INDUSTRY / EMPLOYER EXPECTED OUTCOMES

Use digital andmicroprocessor based systems for various industrial applications.

IV. COURSE LEARNING OUTCOMES

At the end of the course, students will be able to achieve the following course learning outcomes:

CO1. Understand various number systems, inter conversion and different logic gates.

CO2. Build combinational logic circuits.

CO3. Apply sequential circuits in working of digital system.

CO4. Understand the working of A/D and D/A converters.

CO5. Understand the architecture and basics of 8085 microprocessor.

V. THEORY LEARNING OUTCOMES AND ALIGNED COURSE CONTENT:

Name of Unit	Theory Learning outcomes (TLO's) aligned to CO's	Learning Content mapped with Theory Learning outcomes (TLO's) & CO's	Marks	Hours
Unit-1 Number Systems and Logic Gates	**TLO 1.1** Types of number system, interconversion **TLO 1.2** Basic mathematical operations – 1'scomplement, 2'scomplement **TLO 1.3** Binary addition,subtraction,multiplication and division **TLO 1.4** Introductions to codes –weighted codes: BCD code, non weighted codes: Grey code, Excess code **TLO 1.5** Positive logic and negative logic levels **TLO 1.6** Different types of logic gates, symbol and truth table **TLO 1.7** Universal gates - NAND and NOR	**1.1**Conversion numbers from one to another system **1.2** Subtraction using complements **1.3** Binary arithmetical operations. **1.4** Various types of binary codes and its applications **1.5** Differentiate different logic levels **1.6** Truth table of various logic gates **1.7** Different gates using Universal gates	**16**	**12**

Unit-2 Boolean Algebra and Combinational Circuits	**TLO 2.1**Laws of Boolean algebra **TLO 2.2**Demorgan's theorems **TLO 2.3** Simplification of given Boolean equation **TLO 2.4** Boolean expression and logic diagram and vice versa **TLO 2.5** Combinational circuits: half and full adder, half and full subtractor, Multiplexer and Demultiplexer, Encoder and Decoder	**2.1** Laws of Boolean algebra **2.2** Demorgan's theorems **2.3** Application of Boolean algebra **2.4** Logic circuit for a given Boolean expression **2.5** Understanding about various combinational circuits	**11**	**8**
Unit-3 Sequential Circuits	**TLO 3.1** Flip-Flop (FF) circuits: R-S, D, J-K and master slave J-K **TLO 3.2**Shift register: series, parallel, left and right **TLO 3.3**Asynchronous and Synchronous counter (up to Modulo 8)	**3.1** Working of various Flip Flops with the help of truth table **3.2** Working of various types of shift register **3.3** Waveform of Asynchronous and Synchronous counter	**12**	**9**
Unit-4 A to D And D to A Converters	**TLO 4.1**Digital to Analog conversion: Weighted resistor network type, Binary ladder Network type **TLO 4.2**Analog to Digital conversion: Parallel comparator type, Successive approximation type, Counter OR Staircase type	**4.1** Working of various types of D to A converters **4.2** Working of various types of A to D converters	**12**	**9**
Unit-5 Basics of Microprocesso r	**TLO 5.1** Introduction to microprocessor **TLO 5.2** Advantages and disadvantages of microprocessor control **TLO 5.3** Structure of microprocessor, Generalized architecture of microprocessor, functions of each block **TLO 5.4** Functional block diagram of 8085 microprocessor with pin diagram, logical block diagram of 8085 microprocessor-Registers, ALU, serial control section, interrupt section, timing and control section **TLO 2.5** Assembly language	**5.1** Functions of each block ofgeneralize microprocessors **5.2** Advantages and disadvantages of microprocessor control **5.3** Microprocessor architecture with the help of suitable block diagram **5.4** Memory organization of 8085 Microprocessor	**9**	**7**

	Programming of 8085, Addressing Modes, Instruction classification, Instruction formats **TLO 2.6** Basic Assembly Language programming (only simple arithmetic operations addition, subtraction)			

VI. LABORATORY LEARNING OUTCOME AND ALIGNED PRACTICAL			
Sr. No.	**Practical/Laboratory Learning Outcome (LLO)**	**Practical Titles**	**Relevant COs**
1	LLO 1.1: Ability to understand and experimentally verify the operation of basic logic gates and their truth tables.	To study different logic gates and to verify their truth tables.	CO1
2	LLO 1.2: Ability to verify NAND gate as a universal gate by implementing basic logic functions.	To verify NAND gate as UNIVERSAL gate.	CO1
3	LLO 1.3: Ability to verify NOR gate as a universal gate by implementing basic logic functions.	To verify NOR gate as UNIVERSAL gate.	CO1
4	LLO 1.4: Ability to experimentally verify De Morgan's theorems using logic gates.	To verify De Morgan's theorems.	CO2
5	LLO 1.5: Ability to design and implement half adder and full adder circuits and verify their outputs.	To perform half adder and full adder	CO2
6	LLO 1.6: Ability to design and implement half subtractor and full subtractor circuits and verify their outputs.	To perform half subtractor and full subtractor	CO2
7	LLO 1.7: Ability to study and operate a 7-segment LED display using appropriate logic circuits.	To study and perform BCD to 7-Segment decoder.	CO2
8	LLO 1.8: Ability to construct and analyze R-S and D flip-flop circuits used in sequential logic systems.	To build and perform R-S and D flip flop	CO3
9	LLO 1.9: Ability to study and perform the functioning of shift registers for data storage and transfer.	To study and perform the function of shift resister.	CO3
10	LLO 1.10: Ability to understand and demonstrate the working principle of analog-to-digital (A/D) conversion.	To study the analog to digital (A/D) conversion.	CO4
11	LLO 1.11: Ability to understand and demonstrate the working principle of digital-to-analog (D/A) conversion.	To study the digital to analog (D/A) conversion.	CO4
12	LLO 1.12: To be familiar with command keys and memory map of 8085	Introduction to microprocessor programming kit	CO5
13	LLO 1.13:Develop and execute an assembly language programme to perform arithmetic operation.	To develop assembly language programme for addition using 8085.	CO5

VII. SUGGESTED MICRO PROJECT / ASSIGNMENTS / ACTIVITIES FOR SELF LEARNING / SKILL DEVELOPMENT (SELF LEARNING)

Following are the suggested student related co-curricular activities

- Prepare a chart of various logic gates and their truth table.
- Give a seminar on a relevant topic.
- Write assembly language programme for subtraction using 8085.

Mini projects

- Prepare circuit for any application using logic gates.
- Build and test any combinational logic circuit and prepare truth table.
- Design and implement a timer-based buzzer circuit using counters and flip-flops.
- Develop a BCD to 7-segment display interfacing system using decoder logic.
- Design and demonstrate a functional block-level model of the 8085 microprocessor.

VIII. LIST OF INSTRUMENTS / EQUIPMENT / TRAINER BOARD

1	Bread board with connecting wires & various logic input/output facilities
2	Various Logic Gates, Flip-Flop, Registers, Counters, Encoder, Decoder
3	Digital Logic trainer board
4	A/D and D/A trainer modules
5	Universal counter module
6	Digital Multimeter

IX. LIST OF REFERENCE BOOKS

Sr.No.	Title	Author	Publication
1	Digital Electronics	Sanjay Sharma	S.K.Kataria& sons
2	Digital Electronics (for Polytechnics)	Pratima Manhas, Shaveta Thakral	S.K.Kataria& sons
3	Electronic devices & circuits	Allen Mottershed.	Prentice Hall of India
4	Microprocessor Architecture, Programming and Applications with 8085	Gaonkar, Ramesh S.	Penram International Publishing(India)Pvt.Ltd. New Delhi (5thEdition)
5	Fundamentals of Microprocessors and Microcontrollers	Ram, B.	Dhanpat Rai Publications, NewDelhi

X. LINK OF LEARNING WEB RESOURCE

1	**www.nptl.iitm.ac.in**
2	**www.alldatasheet.com**
3	**www.youtube.com/nptelhrd**
4	www.Howstuffworks.com

XI. SUGGESTED WEIGHTAGE TO LEARNING EFFORTS & ASSESSMENT PURPOSE

Unit	Unit Title	Aligned COs	Learning Hours	R-Level	U-Level	A-Level	Total Marks
1	Number Systems and Logic Gates	CO1	12	6	5	5	16
2	Boolean Algebra and Combinational Circuits	CO2	8	4	3	4	11
3	Sequential Circuits	CO3	9	4	4	4	12
4	A to D and D to A Converters	CO4	9	4	4	4	12
5	Basics of Microprocessor	CO5	7	3	3	3	9
		Grand Total	45	21	19	20	60

XII. COs AND POs AND PSOs MAPPING

Course outcome	Programme Outcomes (POs)	Programme Specific Outcomes (PSOs)

(Cos)										
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
CO1	3	2	1	1	1	2	0	3	1	1
CO2	3	2	3	2	1	1	1	2	3	1
CO3	3	3	2	2	1	1	2	3	2	3
CO4	2	2	2	1	2	2	1	1	3	2
CO5	3	2	2	1	3	2	2	3	2	2
Legends: -*3- High*			*2-Moderate/Medium*			*1-Slight/Low*		*0-None*		